Craig B. Agricola

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Profile

Seasoned engineer with experience in positions requiring deep knowledge of software, hardware, development infrastructures, and tools. Seeking challenges that will allow me to learn new tools and solve new types of problems. Co-author of two patents and two academic papers (one winning a "best paper" award).

Technical Proficiencies

C, C++, Perl, Java, Shell (Bash, Bourne, C), SQL, PostScript, Git, Various assembly languages, Verilog, PLI, Linux, Solaris, AIX, Windows, Mac OS

Experience

IBM

Advisory Development Engineer — IBM — Jun 2008 to Jul 2011, Jun 2013 to Present

Responsible for verification of multiple accelerator engines for POWER7+ and POWER9 processors, functions including symmetric encryption, cryptographic hashing, dynamic memory compression, and GZIP compression.

Advisory Development Engineer — IBM — Jul 2011 to Jun 2013

Responsible for command generator and driver for verification of CAPI (Coherent Accelerator Processor Interface) unit on POWER8 processor.

Netronome Systems, Inc

Senior Staff Engineer — Netronome Systems, Inc. — Mar 2008 to Jun 2008

Developed verification components in System Verilog using the Open Verification Methodology to be used in the verification of a network processor based on Intel's IXP28xx line of processors.

Intel

Component Design Engineer — Intel — Jan 2005 to Mar 2008

Developed infrastructure to support pre-silicon platform verification of Intel's Common System Interface (CSI) link technology in the inaugural Itanium microprocessor to use CSI and the supporting I/O Hub (IOH) chipset. As the microprocessor and the IOH chip were written in different design languages, the environment involved two separate simulation environments connected by a software backplane. The specific responsibility was development of the API and mechanism which allowed for communication and synchronization of simulation state information between the two simulators which were on distinct machines. Follow on work was to apply this same API and communication/synchronization mechanism to Intel's second generation of Xeon processor to use CSI. During this work, I became the expert on the software backplane, providing support for many different projects that were using it.

Axiowave Networks

Senior Hardware Engineer — Axiowave Networks — May 2001 to Nov 2004

Built software environment to verify central control chip in core network router. Provided significant input to the architectural design of the chip, and co-authored a patent application covering the use of the central control processor to perform fair sharing of unsubscribed bandwidth.

Senior Hardware Engineer — Axiowave Networks — Aug 2003 to Aug 2004

Architected hardware redundancy scheme for central control chip in core network router. Developed software model to evaluate correctness and performance impact.

Senior Hardware Engineer — Axiowave Networks — Jun 2002 to May 2003

Developed drivers for lab bring-up of central control chip in core network router.

ICLUBcentral

Senior Software Engineer — ICLUBcentral — Sep 2000 to May 2001

Led a two person development team of the software component that provides real-time market data to an online group financial software platform. Wrote the component in Java, which provided services to dynamic web pages written with Mason (Perl), requiring significant interaction with the Oracle database (SQL) for caching market data and complex queries against the data.

IBM

Software Engineer — IBM — Jul 2000 to Sep 2000

Developed the synthesis flow for IBM's G3 PowerPC 750FX processor (Sahara) when it was branched from Gecko, the custom PowerPC chip that powers Nintendo's GameCube. This included taking back-end-of-line fixes from Gecko and inserting them in Sahara, and checking the equivalence of the changes with Verity.

Software Engineer — IBM — Dec 1999 to Jul 2000

Identified optimizations in very long single threaded PowerPC workloads by implementing a distributed system for generating traces. Implemented numerous optimizations for the target processor in GCC.

Software Engineer — IBM — Jul 1999 to Dec 1999

Developed software tools for performance modeling of IBM's Ravina project.

Software Engineer — IBM — Jan 1998 to Jul 1999

Researched dynamic binary translation, culminating in two papers. Developed software that performed dynamic binary translation of PowerPC workloads to a new VLIW architecture leveraging profiled execution path information. This work provided input to the architecture for the VLIW processor BOA (Binary-translation Optimized Architecture).

Software Engineer — IBM — Jun 1997 to Jan 1998

Worked on a very small team to develop the architecture of PowerPCX, a VLIW processor intended to be the high frequency successor to the PowerPC. The ISA was designed to allow direct translation of PowerPC opcodes to a corresponding sequence of fully predicated VLIW instructions. Co-authored a patent was covering the novel load/store architecture.

Summer Pre-Professional — IBM — May 1995 to Aug 1996

Developed software suite to keep a server farm of 400 machines continuously busy with directed random testing of the PowerPC 615.

Publications

Erik Altman, Michael Gschwind, Sumedh Sathaye, Stephen Kosonocky, Arthur Bright, Jason Fritts, Paul Ledak, David Appenzeller, Craig Agricola, Zachary Filan. "BOA: The Architecture of a Binary Translation Processor." IBM Research Report RC 21665, Dec. 2000

Sumedh Sathaye, Paul Ledak, Jay LeBlanc, Stephen Kosonocky, Michael Gschwind, Jason Fritts, Zachary Filan, Arthur Bright, David Appenzeller, Erik Altman, and Craig Agricola. "BOA: Targeting Multi-Gigahertz with Binary Translation." In *Proc. of the 1999 Workshop on Binary Translation, IEEE Computer Society Technical Committee on Computer Architecture Newsletter*, December 1999. Awarded Best Paper.

Education

University of Vermont, Burlington, Vermont
Spring 2016-Present
Ph.D. degree candidate in Computer Science
Cumulative G.P.A.: 4.00.

University of Vermont, Burlington, Vermont
Fall 1999-Fall 2000, Fall 2011-Spring 2015
M.S. degree in Computer Science
Cumulative G.P.A.: 3.90.

Case Western Reserve University, Cleveland, Ohio
1993-1997
B.S. degree in Computer Engineering,
minor in Economics
Cumulative G.P.A.: 3.52.